AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A signal synchronizing circuit for prohibiting signals traveling from a first clock domain operating with a first clock to a second clock domain operating with a second clock when the first clock is not active, the synchronizing circuit comprising:

at least one signal receiving module for receiving at least one selected signal in the first clock domain;

a detection circuit producing a detection signal indicating that the first clock is active; and

at least one output selection module for passing the selected signal from the first clock domain to the second clock domain only when the first clock is active.

2. (Original) The circuit of claim 1 wherein the signal receiving module includes a flip-flop receiving the selected signal upon a triggering of the first clock.

3. (Original) The circuit of claim 1 wherein the output selection module includes a first flip-flop receiving the selected signal from the first clock domain upon a triggering of a gated clock generated by a gated clock module.

4. (Original) The circuit of claim 3 wherein the gated clock module further includes:

a second flip-flop receiving the detection signal upon a triggering of the second

clock; and

an AND gate passing the output of the flip-flop to generate the gated clock when the second clock is active.

5. (Original) The circuit of claim 1 wherein the detection circuit further includes two or more flip-flops arranged in series that are synchronized with the first clock.

6. (Original) The circuit of claim 5 wherein the flip-flops have a constant value for their inputs and the first clock as their clock inputs.

7. (Original) The circuit of claim 5 wherein the detection circuit further includes at least one flip-flop synchronized with the second clock and connected in series with the flip-flop generating the detection signal.

8. (Original) The circuit of claim 1 further comprising a disable circuit for disabling the detection signal when the first clock becomes inactive.

9. (Original) The circuit of claim 8 wherein the disable circuit further includes:

a counter for receiving the detection signal as its input when triggered by the first clock to generate a counter output;

a first multiplexer based sample circuit generating a first sample of the counter output in the second clock domain;

a second multiplexer based sample circuit generating a second sample of the

counter output in the second clock domain;

a comparison module for comparing whether the first and second samples are the same; and

a third multiplexer based sample circuit for generating a disable signal when the first and second samples are the same.

10. (Original) The circuit of claim 9 wherein the first and second multiplexer based sample circuits generate the first and second samples upon a sample triggering signal at a predetermined time for preventing inadvertently disabling the detection signal.

11. (Original) The circuit of claim 10 wherein the disable circuit further includes a check signal asserted for a full second clock after the sample triggering signal is asserted.

12. (Original) A signal synchronizing circuit for allowing signals traveling from a first clock domain operating with a first clock to a second clock domain operating with a second clock, the circuit comprising:

a detection circuit producing a detection signal indicating that the first clock is active; and

a signal synchronization module that allows at least one selected input signal to pass from the first clock domain to the second clock domain when the first clock is active, the signal synchronization module further comprising:

a first latch synchronizing the detection signal with the second clock;

a signal passing module passing the output of the first latch to generate a gated clock signal that is synchronized with the second clock; and

an output selection module for passing the selected input signal upon a triggering of the gated clock signal.

13. (Original) The circuit of claim 12 wherein the detection further includes two or more flip-flops arranged in series that are synchronized with the first clock.

14. (Original) The circuit of claim 13 wherein the flip-flops have a constant value for their inputs and the first clock as their clock inputs.

15. (Original) The circuit of claim 12 wherein the signal passing module is an AND gate.

16. (Original) The circuit of claim 12 further comprising a disable circuit for disabling the detection signal when the first clock is detected as being inactive.

17. (Original) The circuit of claim 16 wherein the disable circuit further includes:

a counter for receiving the detection signal as its input when triggered by the first clock to generate a counter output;

a first multiplexer based sample circuit generating a first sample of the counter output in the second clock domain;

a second multiplexer based sample circuit generating a second sample of the

counter output in the second clock domain;

a comparison module for comparing whether the first and second samples are the same; and

a third multiplexer based sample circuit for generating a disable signal when the first and second samples are the same.

18. (Original) The circuit of claim 17 wherein the first and second multiplexer based sample circuits generate the first and second samples upon a sample triggering signal at a predetermined time for preventing inadvertently disabling the detection signal.

19. (Original) The circuit of claim 18 wherein the disable circuit further includes a check signal asserted for a full second clock after the sample triggering signal is asserted.

20. (Original) A method for prohibiting signals traveling from a first clock domain operating with a first clock to a second clock domain operating with a second clock to be synchronized with the second clock when the first clock is inactive, the method comprising:

receiving at least one selected signal in the first clock domain;

detecting that the first clock is inactive; and

prohibiting the selected signal from the first clock domain to be synchronized with the second clock when the first clock is detected to be inactive.

21. (Original) The method of claim 20 wherein the receiving further includes receiving the selected signal upon a triggering of the first clock using a flip-flop.

22. (Original) The method of claim 20 wherein the prohibiting further includes generating a gated clock signal that prohibits the operation of at least one output selection circuit that receives the selected signal.

23. (Original) The method of claim 22 further includes:

synchronizing the detection signal with the second clock; and

passing the synchronized detection signal to generate the gated clock when the second clock is active.

24. (Original) The method of claim 20 wherein the detecting further includes detecting whether the first clock is inactive by feeding a constant input to at least one flip-flop that is synchronized with the first clock.

25. (Currently Amended) The method of claim 20 further comprising disabling the detection signal when the first clock ~~become~~ becomes inactive.

26. (Original) The method of claim 25 wherein the disabling further includes:

receiving the detection signal as an input of a counter when triggered by the first clock to generate a counter output;

generating a first sample of the counter output by a first multiplexer based

sample circuit in the second clock domain;

generating second sample of the counter output by a second multiplexer based sample circuit in the second clock domain;

comparing whether the first and second samples are the same; and

generating a disable signal by a third multiplexer based sample circuit when the first and second samples are the same.

27. (Original) The method of claim 26 wherein the first and second multiplexer based sample circuits generate the first and second samples upon a sample triggering signal at a predetermined time for preventing inadvertently disabling the detection signal.

28. (Original) The method of claim 27 further includes asserting a check signal for a full second clock after the sample triggering signal is asserted.